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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,072	11/25/2003	Chih-Mu Huang	67,200-1178	5526

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,072	HUANG ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) 22-32 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed on 3/10/2005.

Currently, claims 1-32 are pending. Claims 22-32 are withdrawn from consideration.

Election/Restrictions

1. Claims 22-32 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected device, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 3/10/2005.

2. Applicant's election with traverse of claims 1-21 in the reply filed on 3/10/2005 is acknowledged. The traversal is on the ground(s) that the structure can only be enabled by the method shown. This is not found persuasive because while the method forms the structure this is not the only way to arrive at the structure, so the structure limitations are not bound by or are exclusively formed by the method of the current invention.

The requirement is still deemed proper and is therefore made FINAL.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 5-9, 12, 13 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Leung et al. (U.S. Patent No. 6,468,855 dated 10/22/2002).

Leung shows the method substantially as claimed in, Figs. 3A-3F, and corresponding text as: providing a silicon substrate (306) comprising an STI structure (col. 8, lines 30-34) (314) and an overlying dielectric gate layer (307, 308) (col. 8, lines 14-56); depositing a polysilicon layer (303) (col. 6, lines 14-51); forming a pass transistor structure (303) adjacent a storage capacitor structure (313) separated by a predetermined distance (col. 7, lines 26-45) and (col. 8, lines 35-56); carrying out a first ion implantation process (312) to form first and second doped regions adjacent either side of the pass transistor structure, the first doped region defined by the predetermined distance (col. 8, line 57-col. 9, line 18); depositing a spacer dielectric layer (325) (col. 9, line 19-24); etching back the spacer dielectric layer to leave an unetched spacer dielectric layer portion overlying the first doped region while forming a sidewall spacer of a predetermined width overlying a first portion of the second doped region (Fig. 3E) (col. , lines 9-24); and carrying out a second ion implantation process (311) to form a relatively higher dopant concentration in a second portion of the second doped region (col. 8, line 57-col. 9, line 18) (claim 1). Leung teaches the step of forming self aligned

silicide regions over the second portion, the pass transistor structure and the storage capacitor structure (col. 8, line 57-col. 9, line 18) (claim 2). Leung teaches that the storage capacitor structure is formed at least partially overlying the STI structure (Fig. 3E) (col. 8, line 57-col. 9, line 18) (claim 5). Leung teaches that the predetermined distance is less than about twice the predetermined width (Fig. 3E) (col. 8, line 57-col. 9, line 18) (claim 6). Leung teaches that the spacer dielectric layer thickness is about greater than about half of the predetermined distance (Fig. 3E) (col. 8, line 57-col. 9, line 18) (claim 7). Leung teaches that the pass transistor structure and the storage capacitor structure comprise a memory cell formed over an N doped well region (304) of a P doped silicon substrate (col. 6, line 62-col. 7, line 14) (claim 8). Leung teaches that the first and second doped regions respectively comprise P- and P+ doped regions (col. 8, line 57-col. 9, line 18) (claim 9). Leung shows the method substantially as claimed in, Figs. 3A-3F, and corresponding text as: providing a silicon substrate (306) comprising an STI structure (col. 8, lines 30-34) (314) and an overlying dielectric gate layer (307, 308) (col. 8, lines 14-56); depositing a polysilicon layer (303) (col. 6, lines 14-51); forming a pass transistor structure (303) adjacent a storage capacitor structure (313) separated by a predetermined distance for forming a first doped region (col. 7, lines 26-45) and (col. 8, lines 35-56); carrying out a first ion implantation process (312) to form the first doped region and a second doped region adjacent the pass transistor structure; (col. 8, line 57-col. 9, line 18); blanket depositing a spacer dielectric layer (325) (col. 9, line 19-24); etching back the spacer dielectric layer to leave an unetched spacer dielectric layer portion overlying the first doped region while forming a sidewall spacer of

a predetermined width overlying a first portion of the second doped region (Fig. 3E) (col. , lines 9-24); and carrying out a second ion implantation process (311) to form a relatively higher dopant concentration in a second portion of the second doped region (col. 8, line 57-col. 9, line 18) (claim 12). Leung teaches the step of forming silicide regions over the second portion, the pass transistor structure and the storage capacitor structure (col. 8, line 57-col. 9, line 18) (claim 13). Leung teaches that the storage capacitor structure is formed at least partially overlying the STI structure (Fig. 3E) (col. 8, line 57-col. 9, line 18) (claim 16). Leung teaches that the predetermined distance is less than about twice the predetermined width (Fig. 3E) (col. 8, line 57-col. 9, line 18) (claim 17). Leung teaches that the pass transistor structure and the storage capacitor structure comprise a memory cell formed over an N doped well region (304) of a P doped silicon substrate (col. 6, line 62-col. 7, line 14) (claim `8). Leung teaches that the first and second doped regions respectively comprise P- and P+ doped regions (col. 8, line 57-col. 9, line 18) (claim 19).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (U.S. Patent No. 6,468,855 dated 10/22/2002).

Leung shows the method substantially as claimed and as described in the preceding paragraph.

Leung lacks anticipation only in not explicitly teaching that: 1) the first doped region is doped to a level of between about 10^{12} and 10^{14} dopant atoms/cm^2 and the second doped region comprises a relatively higher doped region of greater than about 10^{15} dopant atoms/cm^2 (claims 10 and 20).

Leung shows in a different embodiment is formed in p-type source region (44) at an implant dosage about $10^{14}/cm^2$. Leung also shows the p+ type dopant (417) that is implanted with a dosage of about $10^{16}/cm^2$. The invention is used to improve soft-error rate sensitivity of DRAM cell, to minimize the sub-threshold leakage.

It would have been obvious to one of ordinary skill in art, at the time the invention was made, to modify the method shown in Leung, such that the first doped region is doped to a level of between about 10^{12} and 10^{14} dopant atoms/cm^2 and the second doped region comprises a relatively higher doped region of greater than about 10^{15} dopant atoms/cm^2, as taught by Leung, with the motivation that Leung teaches improved soft-error rate sensitivity of DRAM cell, to minimize the sub-threshold leakage.

9. Claims 3, 11, 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (U.S. Patent No. 6,468,855 dated 10/22/2002) in view of Tzeng et al. (U.S. Patent No. 6,670,664 filed 10/22/2002).

Leung shows the method substantially as claimed and as described in the preceding paragraph.

Leung lacks anticipation only in not explicitly teaching that: 1) the dielectric gate layer is selected from the group consisting of SiO_2, nitrided SiO_2, and oxide/nitride (claims 3 and 14); and 2) the spacer dielectric layer comprises one or more layers selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride (claims 11 and 21).

Tzeng shows the single transistor random access memory cell with dual threshold voltages. The dielectric layer (14a, b, c) is formed of a silicon oxide (col. 4, lines 9-17). The spacer layers (26 a, b, k, l) are formed are formed of silicon nitride (col. 6, lines 32-40). It is desirable for additional single transistor random access memory cell structures with enhanced performance and to control differences with the threshold voltage (col. 1, lines 52-53) (col. 2, lines 29-42).

It would have been obvious to one of ordinary skill in art, at the time the invention was made, to modify the method shown in Leung, such as the dielectric gate layer and spacer are formed of silicon oxide and silicon nitride respectively, as taught by Tzeng, with the motivation that Tzeng teaches that enhanced performance and to control differences with the threshold voltage.

10. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (U.S. Patent No. 6,468,855 dated 10/22/2002) in view of Mizushima et al. (U.S. Patent No. 6,395,621 dated 5/28/2002).

Leung shows the method substantially as claimed and as described in the preceding paragraph.

Leung lacks anticipation only in not explicitly teaching that: 1) the dielectric gate layer comprises material selected from the group consisting of Ta2O5, TiO2, HfO2, Y2O3, La2O5, ZrO2, BST, and PZT (claims 4 and 15).

Mizushima shows a semiconductor device with an oxide mediated epitaxial layer. In Fig. 13 D a gate oxide (16) is formed this oxide is made of tantalum oxide (col. 17, line 65-col. 18, line 3). This overcomes the problem of large leakage current between the silicon substrate and the S/D region.

It would have been obvious to one of ordinary skill in art, at the time the invention was made, to modify the method shown in Leung, such as the dielectric gate layer comprises material selected from the group consisting of Ta2O5, TiO2, HfO2, Y2O3, La2O5, ZrO2, BST, and PZT, as taught by Mizushima, with the motivation that Mizushima solves the problem of large leakage current between the silicon substrate and the S/D region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
May 24, 2005